REMARKS

Claims 1-7, 9-10, and 13-20 will remain pending in the current Application upon entering this Amendment. Claims 1, 6, 9, 10, and 18 have been amended; and claims 8, 11, and 12 have been cancelled. Applicant submits that the amendments do not add new matter to the current Application. Applicant also submits that (1) no amendment made was related to the statutory requirements of patentability unless expressly stated herein, and (2) no amendment made was for the purpose of narrowing the scope of any claim, unless Applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Drawings

The Examiner states that Figure 1 should be designated by a legend such as –Prior Art- because only that which is old is illustrated. The Examiner proceeds to state that it is the same figure as FIG. 1 in US Patent 5,923,893 (Moyer). Applicant respectfully disagrees. That is, the elements of FIG. 1 in the current application differ from those of FIG. 1 in Moyer. For example, these differences are explained in reference to FIGs. 2-9 where many of the blocks are further explained. For example, the processor and coprocessor of FIG. 1 of the current Application differs from the processor coprocessor of FIG. 1 of Moyer in that new elements and signals are introduced which are described in more detail in reference to subsequent figures (see, e.g., FIG. 2 which further illustrates processor 12 and FIG. 3 which further illustrates coprocessor 14). Therefore, it is incorrect to state that FIG. 1 of the current Application only illustrates that which is old simply because it looks like another figure of another patent, because the differences within the system of FIG. 1 are not illustrated in more detail until subsequent drawings. Therefore, Applicant submits that it is incorrect to label Fig. 1 as prior art.

The Examiner objects to the drawings under 37 CFR 1.83(a) because the Examiner submits that the drawings do not show the features specified in claims 6, 7, 8, 17, and 20. However, Applicant respectfully disagrees. The drawings show each of the features where the functionality of the illustrated features are described in the specification. However, although Applicant believes additional drawings are not required in the current Application, Applicant has added FIGs. 10 and 11 only to further prosecution and not because Applicant agrees with the

drawing objections. (Note also that claim 8 was cancelled, therefore the objection to the features of claim 8 is now moot.)

With respect to claims 6 and 7, Applicant has added a flow diagram as FIG. 10 clearly illustrating the method. Applicant submits that FIG. 10 adds no new matter since it simply reflects the information that was originally presented in claims 6 and 7. Furthermore, it adds no new matter because the written description clearly describes the aspect of a region indicator (e.g. H_REGION 128 described throughout the written description provided from processor 12 to, e.g., processor 14, see also page 18, lines 8-15) and the aspect of "selectively altering an execution mode ... in response to the region indicator" (e.g. see page 21, lines 1-19). Furthermore, block 204 of FIG. 10 also states "wherein altering the execution mode of the first processor may include altering a functionality of the first processor" which is clearly supported by claim 7. This aspect is also described in the written description on pages 21 and 22.

With respect to claim 17, Applicant has added FIG. 11 which includes a portion of broadcast region control unit 120 in accordance with an alternate embodiment where the broadcast regions are defined using base locations and masks. Applicant submits that FIG. 11 adds no new matter since it simply reflects the information that was originally presented in claim 17. Furthermore, it adds no new matter because the written description clearly describes this alternative embodiment of broadcast region control unit 120. For example, as described in reference to FIG. 9, the broadcast regions may be defined with upper and lower bounds. However, as described in the specification on page 20, line 17, to page 21, line 4, other embodiments may be used within broadcast region control unit 120 to define broadcast regions, such as with a base location and a mask.

With respect to claim 19, the Examiner sates that "...selectively providing said operand to be written to said one of the plurality of registers during said write operation based on the current execution region" is not shown in the Figures. However, Applicant respectfully disagrees. For example, this feature is clearly showed with respect to FIG. 7 where it can be seen that, based on different execution regions (for H_REGION[N:1] 128 = '1' or '2'), operands to be written to one of a plurality of registers is selectively provided via HDP[31:0] 72. Firstly, note that broadcast regions may be referred to as execution regions (see page 21, lines 7-8), therefore, H_REGION applies to both broadcast regions and execution regions. Referring to FIG. 7, the result of ADD R3, R2 is written to R3, and since mask 1 158 (corresponding to

REGION '1' 164 where H_REGION is '1') indicates that writes to R3 should be broadcast via HDP 72, it is provided via HDP 72 (as illustrated by the "result of ADD" which appears that cycle. However, the result of OR R4, R5 is not provided because mask 1 indicates that writes to R4 should not be broadcast. Similarly, note that when the current execution region is a different region, such as when H_REGION is '2' (shown in the second portion of FIG. 7 corresponding to REGION '2' 166), only the results of the AND R6, R7 and MUL R9, R10 are broadcast due to the information provided in MASK 2 160. Therefore, depending on the execution region, writes to certain registers are provided. For example, operands written to R3 are provided via HDP when in region '1' 164 but not when in region '2' 166. See also pages 16 and 17 for further descriptions of FIG. 7.

With respect to claim 20, since execution regions may also be referred to as broadcast regions, the features of "wherein each execution region .... for defining the execution region" is clearly illustrated in reference to FIG. 9, which defines regions by upper and lower bounds, and in reference to FIG. 11, which defines regions by base location and mask. Therefore, Applicant submits that claims 19 and 20 are clearly illustrated in the drawings.

Specification

With respect to the title, Applicant submits that the title is descriptive; however, Applicant is amending the title to: METHOD AND APPARATUS FOR INTERFACING A PROCESSOR TO A COPROCESSOR IN WHICH THE PROCESSOR IS CAPABLE OF SELECTIVELY BROADCASTING TO OR SELECTIVELY ALTERING AN EXECUTION MODE OF THE COPROCESSOR. Applicant submits that this new title is also clearly indicative of the invention to which the claims are directed.

Applicant has also added text to Brief Description of the Drawings and Detailed Description to describe added FIGs. 10 and 11. Applicant submits that no new matter has been added to the current Application (as discussed above with respect to the added FIGs.).

Respecting Examiner's request that Applicant includes a *Summary of Invention*, Applicant respectfully points out that (1) 37 CFR 1.77(b) states "The specification *should* include the following sections in order: [(b)(1) through (b)(11)]," (wherein (b)(6) is Brief Summary of the Invention); and (2) both 37 CFR 1.73 and the MPEP 608.01(d) state, "Such

summary [of the Invention] should, *when set forth* be commensurate with the invention as claimed and any object recited should be that of the invention as claimed." Applicant accordingly submits that both Title 37 of the Code of Federal Regulations (CFR) and the Manual of Patent Examining Procedure (MPEP) unambiguously state, by using the word *should* and not *must,* that the Brief Summary of the Invention is optional with respect to its use in U.S. Patent Applications. Accordingly, because Federal Law does not so require, Applicant chooses not to include a Summary of the Invention in the current Application.

Claims Objections

The Examiner has objected to claim 18 since claims 18 recites "the compare circuitry". Applicant has amended claim 18 to replace "compare circuitry" with "execution region control unit". Therefore, Applicant believes to have addressed the Examiner's claim objections.

Claim Rejections

Applicant respectfully submits that claim 1-5 and 9 are patentable under 35 U.S.C. 102(b) over *Supporting Systolic and Memory Communication in iWarp* (hereinafter referred to as Borker). With respect to claim 1, Applicant has amended claim 1 to further clarify "selectively providing ... based on the broadcast specifier." Therefore, claim 1 further includes "wherein said operand is provided to said coprocessor communication bus when the broadcast specifier indicates that broadcasting is enabled and said operand is not provided to said coprocessor communication bus when the broadcast specifier indicates that broadcasting is not enabled." Applicant submits that this is not taught or suggested by Borker. The Examiner states that the set of message queues is the broadcast specifier (page 5, lines 5-6, of the current Office Action) and further states that "to selectively broadcast via a coprocessor communication bus *is to select an output logical channel to transmit data to a different cell*" (page 5, lines 17-18, of the current Office Action). On page 6, in item c, the Examiner, referring to 7.1 of Borker, describes that the operand is written to the result register which is the output systolic gate and the result is then queued for transmission to another cell. The Examiner then states: "Selectively providing via said coprocessor communication bus said operand *is the transmission of the operand from one*

source cell to the destination cell. The result enters and is eventually transmitted from one message queue selected from the broadcast specifier, the set of message queue. The destination of the transmission based on the message queue." However, selectively providing, as claimed in claim 1, is not simply selecting an output logic channel or transmitting an operand from one source to the destination cell, as described by Borker. That is, claim 1 includes providing the operand or not providing the operand to the coprocessor based on the broadcast specifier. However, in Borker, once the operand is written to the results gate (the output gate), it will get queued out to the message queue that is associated with the logical channel bound to the gate (see, e.g. section 7.1 of Borker). That is, the operand *will* get sent out from the message queue to the corresponding destination. The message queue does not determine whether or not it is even sent out, as claimed in claim 1. Furthermore, Borker does not teach or discuss any broadcast specifier which is used to determine whether or not an operand is provided via a coprocessor communication bus. Therefore, for at least these reasons, Applicant submits that claim 1 is patentable over Borker.

Claims 2-5 have not been independently addressed since they depend directly or indirectly from allowable claim 1 and are therefore also allowable for at least those reasons provided above with respect to claim 1.

With respect to claim 9, Applicant has amended claim 9 to further clarify "selectively providing ... based on a current execution region of said processor." Therefore, the "selectively providing" further includes "determining whether broadcast is enabled for the current execution region, if broadcast is enabled for the current execution region, providing said operand via said coprocessor communication bus, and if broadcast is not enabled for the current execution region, not providing said operand via said coprocessor communication bus. " Applicant submits that this is not taught or suggested by Borker. The Examiner states the feature of current execution regions is deemed inherent in Borker because "the cells in iWarp are programmed individually with explicit communication directives, and thus each cell has its own program code to run." The Examiner then states that "the transmission (selectively providing via said coprocessor communication bus said operand to be written in said register file) is based on the individual cell's program code (the current execution region of said processor)." Firstly, as described above in reference to claim 1, Borker does not teach or discuss "selectively providing an operand" by determining whether or not an operand is provided via coprocessor bus. That is, "selectively

providing" in claim 9 does not only refer to the transmission of an operand, but includes determining whether or not to even transmit the operand. Furthermore, in claim 9, this determination of whether or not to provide the operand is based on a current execution region of the processor. Note that Applicant has also amended claim 9 to include "wherein the current execution region of said processor indicates a section of program code that is currently being executed." The Examiner states that the individual cell's program code is the current execution region of said processor, however the cell's program code does not provide information as to the *current execution* region. Furthermore, Borker does not teach providing or not providing an operand based on what section of the program code within the cell is currently being executed. Therefore, for at least these reasons, Applicant submits that claim 9 is patentable over Borker.

Applicant respectfully submits that claim 6 and 7 are patentable under 35 U.S.C. 102(b) over *iWarp: An Integrated Solution to High-Speed Parallel Computing* (hereinafter referred to as iWarp). Applicant has amended claim 6 to clarify that the current execution region indicates "a section of program code that is currently being executed." The Examiner states that the open pathway marker of iWarp teaches the region indicator. However, the open pathway marker of iWarp does not indicate a section of program code that is currently being executed, as claimed in claim 6. The open pathway markers of iWarp provide a way to establish a new pathway from one iWarp cell to another iWarp cell, but does not indicate a current execution region of an iWarp cell, as claimed in claim 6. Therefore, for at least these regions, Applicant submits that claim 6 is patentable over iWarp. Claim 7 depends from claim 6 and is therefore also allowable for at least those reasons which apply to claim 6.

Applicant respectfully submits that claims 10-12 are patentable under 35 U.S.C. 102(b) over US Patent No. 5117350 (hereinafter referred to as Parrish). Applicant has amended claim 10 to include the broadcast indicators of claim 12 and to further clarify that each broadcast indicator corresponds to a register of the plurality of registers and indicates whether or not a write to the corresponding register is to be broadcasted. Applicant have also clarified that the compare circuitry compares the one of the plurality of registers (the one receiving the operand) to a corresponding broadcast indicator wherein the provided broadcast enable signal indicates whether or not broadcasting is enabled for the one of the plurality of registers. The at least one coprocessor communication bus signal therefore provides the operand when the broadcast enable signal enables broadcasting and does not provide the operand when the broadcast enable signal

does not enable broadcasting. Applicant submits that Parrish does not teach or suggest any of these elements.

For example, the Examiner states that each partition RAM is a set of broadcast specifiers. Then, in discussing claim 12, the Examiner states that the fourteen most significant bits of the address providing by the partition RAM entry is the broadcast indicator because they correspond to memory blocks (which the Examiner has indicated as being the plurality of registers). However, the fourteen most significant bits simply provide an address translation of a particular location in memory 314 and do not indicate whether or not an operand written to particular locations in memory 314 is to be broadcast via interconnect bus 360 or not. For example, once a write occurs to a memory location within the DCM portion, it gets provided to system memory with a corresponding translated address, which is provided by local to system partition RAM 319. However, the address translation provided by RAM 319 does not provide a set of broadcast indicators as claimed in claim 10. Furthermore, the Address Translation Hardware 319 (which the Examiner has indicated as being the compare circuitry) does not compare the one of the plurality of registers to a corresponding broadcast indicator within a selected one of the broadcast specifiers, as claimed in claim 10. That is, the Address Translation Hardware 319 provides the fourteen most significant bits and does not compare those bits to the one of the plurality of registers receiving the operand. Therefore, Parrish also does not teach or suggest the compare circuitry or generating the broadcast enable signal as claimed in claim 10. Therefore, for at least these reasons, Applicant submits that claim 10 is allowable over Parrish. Note that Applicant has canceled claims 11 and 12.

Applicant respectfully submits that claims 10 and 13-20 are patentable under 35 U.S.C. 102(b) over US Patent No. 5,485,624 (hereinafter referred to as Steinmetz). With respect to claim 10, Applicant, as described above, has amended claim 10 to include the concept of broadcast indicators from dependent claims 11 and 12. Therefore, Applicant submits that claims 10, as amended, is not taught or suggested by Steinmetz. Note that the Examiner also agrees that claims 11 and 12 are not taught or suggested by Steinmetz, since these claims were not included in the Steinmetz rejections. Claims 13-17 all depend directly or indirectly from allowable claim 10 and are therefore also allowable over Steinmetz for at least those reasons which apply to claim 10.

With respect to claim 18, Applicant has amended claim 18 to further clarify that each of the execution regions indicate a range of instruction addresses. Referring to claim 18, the Examiner, on page 18 (in paragraph c) of the current Office Action, states that "Different combinations of A17-A19, define the execution regions," where the "control signals 29, through the individual assertion of Snoop1 – Snoop3 inputs, indicate when A17-A19 (the indicated address location from the program counter unit) falls within one of a set of execution regions (defined by the selected combinations of A17-A19)." However, Applicant respectfully disagrees with these comments. Firstly, A17-A19 of Steinmetz correspond to *unused* portions of address lines A0-A31 that are used to communication to DMA co-processor 11. (See, e.g., col. 3, lines 5-10, of Steinmetz). Therefore, A17-A19 do not indicate ranges of instruction addresses because these address lines are actually unused address lines. That is, as the values of A17-A19 change, the address location indicated does not because they are not used as address lines. Furthermore, Snoop1 – Snoop3 inputs do not indicate when A17-A19 falls within one of a set of execution regions. Firstly, there is no teaching or suggestion of execution regions in Steinmetz as claimed in claim 18. Secondly A17-A19 do not indicate an address location from the program counter, as stated by the Examiner, since A17-19 are unused address lines and thus cannot indicate values of the program counter since the program counter indicates actual addresses. Therefore, Steinmetz does not teach or suggest an execution region control unit as claimed in claim 18.

Also, with respect to paragraph e on page 19 of the Office Action (still referring to claim 18), Applicant submits that a current execution region from the set of execution regions is *not* the region defined by the address on Address Bus 13, as stated by the Examiner. As discussed above, A17-A19 do not provide for different execution regions, thus the address on Address Bus 13 does not provide a current execution region from the set of execution regions. Therefore, for at least these reasons, Applicant submits that claim 18 is allowable over Steinmetz. Claims 19 and 20 depend directly or indirectly from allowable claim 18 and are therefore also allowable for at least those reasons which apply to claim 18.

Conclusion

Although Applicant may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicant is not discussing all these statements in the current Office Action, yet reserve the right to address them at a later time if necessary.

Applicant respectfully solicits allowance of the pending claims. Contact me if there are any issues regarding this communication or the current Application.

Respectfully submitted,

By: 

Joanna G. Chiu
Attorney of Record
Reg. No.: 43,629
Telephone: (512) 996-6839
Fax No.: (512) 996-6854
Email: Joanna.Chiu@Freescale.com

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
Law Department

Customer Number: 23125